SRINIVAS K (vaasu)

7005 Century Ave, Mississauga, Toronto ● 647 293 2329 ● ksr.iitg@gmail.com ● Webpage

PROFESSIONAL SUMMARY

- Bachelor's in Electronics from Indian Institute of Technology with 7 years of experience in hardware design of complex telecom products
- Experienced with all phases of product life cycle, right from concept to prototyping to mass manufacturing
- Experienced in designing high speed, high density, complex multilayer PCB designs
- Proficient in High-Speed Digital Design involving microprocessors, L2/L3 switch, FPGA, memory interfaces, PCIe and Ethernet Interfaces (1G/10G, 40G & 100G)
- Hands on experience in board bring up, testing and troubleshooting of electronic circuit boards, environmental and EMC/EMI certification of the products
- Experienced in designing complex telecom boards involving ADSL, SONET/SDH, Ethernet and OTN technologies
- Well versed with ITU-T and IEEE standards
- Highly proficient in Printed Circuit Board (PCB) layout concepts and well versed with associated softwares (like Altium Designer, Cadence Allegro) for PCB design and also simulation softwares for performing SI and PDN analysis.
- Experienced with diagnostic equipments like real-time oscilloscopes, spectrum analyzers, logic analyzers, multi meter.
- Team player with excellent written and verbal communication skills
- A disciplined approach to the task at hand and ability to learn new skills quickly
- Ranked amongst the top 1% of test takers in the prestigious IIT-JEE examination held nationwide

SKILL SET

Programming Languages	:	VHDL, C
Simulation Tools	:	Pspice, ADS, Hyperlynx SI/PI
Software Tools	:	Xilinx ISE, Altera Quartus, Cadence Allegro, Altium Designer, XJTAG
Hardware Tools	:	Oscilloscope, Logic Analyzer, SONET/SDH Network tester, Spectrum Analyzer, Optical Network Tester (OTU3/OTU4)

EMPLOYMENT HISTORY

Senior Research Engineer, Next Generation Networks, C-DOT, INDIA (2009 - 2016)

- Worked in various projects like 4 CDC ROADM, VoIP Phone, Gigabit Interface Router and Media Gateway which were customized to defense sector needs
- Authored documents- hardware requirements, design specifications, circuit design and test plan by working in co-ordination with managers and marketing groups
- Led the designs of a Multi layer PCB's which hosts the marvell microprocessor (ARM based) and a ecosystem of Memory modules (flash, DDR3), FPGA and other peripheral interfaces
- Designed and reviewed layer stackup of Multi layer PCBs
- Optimized component selection towards new designs based on functional, environmental and compliance requirements
- Designed Schematics, schematics entry, component creation, layout and routing in Cadence(OrCAD) Allegro tool and design verification
- Designed schematics of Linear and switching power supply design
- Performed high speed signal integrity(SI) analysis with PCB extraction and simulation using ADS

- Worked in closely with PCB layout designer and manufacturers to assure that the product meets the DFT/DFM requirements
- Prepared bill of materials, tested and debugged various hardware by working in closely with software and mechanical design groups
- Programming of various ASICs, VHDL code development, Integration with software, EMI/EMC certification, field deployment and transfer of technology to third party
- Experienced with JTAG, RS232, USB, RS485, Ethernet, I2C, SMI, SPI communication protocols
- Authored several technical manuals and operating procedures for products

Research Intern, NOKIA RESEARCH CENTER, Beijing, CHINA (2008)

- Development of an isolated word recognizer for NATO phonetic alphabet

EDUCATION

Bachelor of Technology in Electronics & Communication Engineering **(2005-2009)**
Indian Institute of Technology-Guwahati (IITG), INDIA
(*Equivalent to Bachelors in Electronics Engineering, CANADA*)(*As Evaluated by WES*)

TRAININGS/CERTIFICATIONS

- "Mastering the SerDes-channel design: 8Gbps PCIe-Gen3 & 16Gbps" by Dr.Hany Fahmy
- 2 day workshop of "Best Design Practices for Signal Integrity" by Dr.Eric Bogatin
- 5 day training on "FPGA based System Design: A System on Chip (SoC) Approach" by C-DAC
- "ESD awareness and control" training by Indian ESD Association

AWARDS/ACHEIVEMENTS

- Ranked amongst the top 1% of test takers in the prestigious IIT-JEE examination held nationwide
- Achieved best bi-annual performance appraisal in C-DOT for past 4 years
- Organized the Techniche'07, the national level technical symposium conducted by IIT Guwahati, by working in close coordination with Marketing, Publicity and Logistics teams

INTERESTS

- IEEE Member
- Avid Yoga Practitioner
- Volley ball, badminton, cycling, travelling